AMENDMENTS TO THE SPECIFICATION

Please amend the specification to read as follows. The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE paragraph [0052] with the following amended paragraph:

[0052] The first switching circuit 51 of the selection part 50 has three FETs 52-54. ~~A drain pin of each FET is~~ A source pin of the FET 52 and each drain pin of the FETs 53 and 54 are respectively connected to the TOVER* pin, the DXN pin, and the DXP pin of the monitoring circuit 11. Hereinafter, to describe the present invention in detail, an FET 52 having a ~~drain~~ source pin connected to the TOVER* pin of the MAX6512 12 of the monitoring circuit 11 is referred to as a "third FET", an FET 53 having a drain pin connected to the DXN pin of the MAX6512 12 of the monitoring circuit 11 is referred to as a "fourth FET", and an FET 54 having a drain pin connected to the DXP pin of the MAX6512 12 of the monitoring circuit 11 is referred to as a "fifth FET".

Please REPLACE paragraph [0053] with the following amended paragraph:

[0053] Respective gates of the third FET 52, the fourth FET 53, and the fifth FET 54 receive a MAX_Q* signal from the switching control circuit 58 (to be described later). A ~~source~~ drain pin of the third FET 52 is connected to a gate of the first FET 15 of the power cut-off circuit 13, and each source pin of the fourth and fifth FETs 53 and 54 is connected to the temperature sensor 7. Herein, the fourth FET 53 regulates the THRMDC signal inputted from the temperature sensor 7 to the DXN pin of the MAX6512 12. The fifth FET 54 regulates the THRMDA signal outputted from the DXP pin of the MAX6512 12 to the temperature sensor 7.

Please REPLACE paragraph [0056] with the following amended paragraph:

[0056] Hereinafter, with the configuration of circuits shown in FIGS. 2 through 4, a control process of the ~~compute~~ computer according to the present invention will be described with reference to FIG. 5.

Please REPLACE paragraph [0060] with the following amended paragraph:

[0060] In the interim, when the POST by the BIOS is ended (S12), the BIOS changes the THRM_SEL signal inputted into the ~~CLR pin~~ CLK pin of the second D flip-flop 59 of the switching control circuit 58 through the South Bridge 3 to “high”. Herein, each signal of the CLR pin, the PR pin and the D pin of the second D flip-flop 59 is maintained “high”, the SIO_Q signal outputted from the Q pin is changed to “high”, and the MAX_Q* signal outputted from the Q* pin is changed to “low”. Herein, the MAX_Q* signal changed to “low” turns off the first switching circuit 51 (S13). Thus, the monitoring circuit 11 has a connection with neither the temperature sensor 7 nor the power cut-off circuit 13.